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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,486	12/15/2003	Daniel Wang	669-77 CON/CIP	3800

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EXAMINER	
WARREN, MATTHEW E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,486	WANG, DANIEL	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-22 and 26-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22 and 26-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on December 21, 2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 31-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 31 and 32 recites the limitation "said insulated bond wires" in line 1 of each claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 26-30 are rejected under 35 U.S.C. 102(a) as being anticipated by Murakami et al. (US 5,866,948).

In re claim 26, Murakami et al. shows (figs. 4, and 10-12) an integrated circuit package comprising a substrate (1) element having first and second opposed surfaces;

a plurality of terminal pads (13 or 28 in fig. 10) disposed on a peripheral portion of the first opposed surface and a plurality of connectors (14) disposed on a peripheral portion of the second opposed surface to define an array of pairs; each pair comprising a terminal pad (13) and a connector (14) in alignment with one another, and an electrically conducting via (12) interconnecting the terminal pad to the connector, the electrically conducting via comprising a pair of straight walls interconnecting the first and second opposed surfaces; a semiconductor chip mounted (2) in a central portion of the first opposed surface, a semiconductor chip comprising a plurality of bond pads (connected to wires 7) on a surface thereof; and a plurality of bond wires (7), each bond wire interconnecting a bond pad on the semiconductor chip to a terminal pad (13) on the substrate element.

In re claims 27-30, Murakami et al. shows (figs. 4 and 10-12) and discloses (col. 4, line 57 – col. 5, line 15) that the substrate (1) is configured to contain a minimal number of layers that reduce inductance, crosstalk, capacitance, etc. The substrate is a single layer substrate and contains no lead frames. The opposite side of the substrate contains a ball grid array (solder connects to lands 14) and each of the terminal pads connects to the balls of the grid array through vias (12) directly traversing the substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US 5,866,948) in view of Kimura (US 5,396,104)

In re claim 13, Murakami et al. shows (figs. 4, and 10-12) an integrated circuit package comprising: (a) a substrate (1) devoid of horizontal traces (col. 4, line 57 – col. 5, line 15), said substrate having terminal pads (13 or 28) arranged along a perimeter of a surface of said substrate (see fig. 10 also); (b) electrically conductive via (12) connecting said terminal pads directly to connectors aligned with the terminal pads (14) on an opposite side of said substrate; (c) a semiconductor chip (2) mounted on the substrate, inside said perimeter, said chip having bond pads (connected to wires 7) located on a surface of said chip; and (d) a plurality of bond wires (7), each of said bond wires extending from a bond pad on said chip to a terminal pad on said substrate. Murakami shows all of the elements of the claims the bond wires being insulated bond wires. Kimura discloses forming high quality insulated bond wires with a thin insulating coating and uniform thickness (col. 6, lines 39-44). The insulated wires used in the semiconductors have excellent insulating and bonding properties making the semiconductors using the wires highly reliable and easily manufactured (col. 13, lines 42-53). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wires of Murakami by using insulated bond wires as taught by Kimura to produce reliable semiconductor devices that are easy to manufacture.

In re claims 14-17, Murakami et al. shows (figs. 4 and 10-12) and discloses (col. 4, line 57 – col. 5, line 15) that the substrate (1) is configured to contain a minimal

number of layers that reduce inductance, crosstalk, capacitance, etc. The substrate is a single layer substrate and contains no lead frames. The opposite side of the substrate contains a ball grid array (solder connects to lands 14) and each of the terminal pads connects to the balls of the grid array through vias (12) directly traversing the substrate.

Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US 5,866,948) in view of Kimura (US 5,396,104) as applied to claim 13 above, and further in view of Bockelman et al. (US 5,471,010).

In re claims 18-20, Murakami in view of Kimura show all of the elements of the claims except the bond wires extending between the bond pads and terminal pads and being positioned to reduce parallelism between adjacent wires. Bockelman et al. shows (figs. 3-5) that insulated bond wires are positioned in a cross-over or twisted arrangement to reduce crosstalk in a circuit (col. 3, lines 12-33). The bond wires are attached in an X in line pattern as seen in fig. 3. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the wire pattern of Murakami in view of Kimura by crossing the wires in an X pattern as taught by Bockelman to reduce crosstalk in the device.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US 5,866,948) in view of Kimura (US 5,396,104) as applied to claim 13 above, and further in view of Murdoch (US 4,002,282).

In re claims 21 and 22, Murakami in view of Kimura show all of the elements of the claims except the bond pad located in an interior portion of a surface of a chip. Although it is well known in the art to form bond pads in any desired configuration or pattern including a pad formed in the center of a chip, Murdoch shows (fig. 1) a method of attaching an insulated bond wire to a bond pad located in an interior portion of the surface of the chip. None of the references specifically disclose that the bond pad is electrically connected to a power or ground connection but it is well known in the art that bond would provide one of a power, ground, or I/O signal connection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the bond pad configuration of Murakami and Kimura by forming a bond pad in the interior of the chip because Murdoch teaches that it is well known in the art to form a bond pad pattern in such a desired configuration.

Claims 31-33, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US 5,866,948) as applied to claim 26 above, and further in view of Bockelman et al. (US 5,471,010).

In re claims 31-33, Murakami shows all of the elements of the claims except the bond wires extending between the bond pads and terminal pads and being positioned to reduce parallelism between adjacent wires. Bockelman et al. shows (figs. 3-5) that insulated bond wires are positioned in a cross-over or twisted arrangement to reduce crosstalk in a circuit (col. 3, lines 12-33). The bond wires are attached in an X in line pattern as seen in fig. 3. Therefore it would have been obvious to one of ordinary skill in

the art at the time the invention was made to modify the wire pattern of Murakami by crossing the wires in an X pattern as taught by Bockelman to reduce crosstalk in the device.

Claims 34 and 35, as far as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami et al. (US 5,866,948) as applied to claim 26 above, and further in view of Murdoch (US 4,002,282).

In re claims 34 and 35, Murakami shows all of the elements of the claims except the bond pad located in an interior portion of a surface of a chip. Although it is well known in the art to form bond pads in any desired configuration or pattern including a pad formed in the center of a chip, Murdoch shows (fig. 1) a method of attaching an insulated bond wire to a bond pad located in an interior portion of the surface of the chip. None of the references specifically disclose that the bond pad is electrically connected to a power or ground connection but it is well known in the art that bond would provide one of a power, ground, or I/O signal connection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the bond pad configuration of Murakami by forming a bond pad in the interior of the chip because Murdoch teaches that it is well known in the art to form a bond pad pattern in such a desired configuration.

Response to Arguments

Applicant's arguments with respect to claims 13-22 and 26-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Loo (5,637,920) shows (fig. 1A) at least one layer of a multi-layered substrate having a chip connected to the substrate and not having any horizontal traces . Pasch (US 5,347,162) is particular relevant in that figures 7-8 show a chip formed on a substrate not having any horizontal traces and vias are formed in a partially vertical or sloped configuration.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
March 4, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER